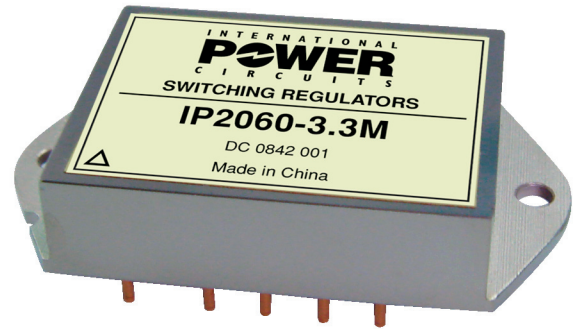




## IP2060 Series Switching Regulators

### FEATURES

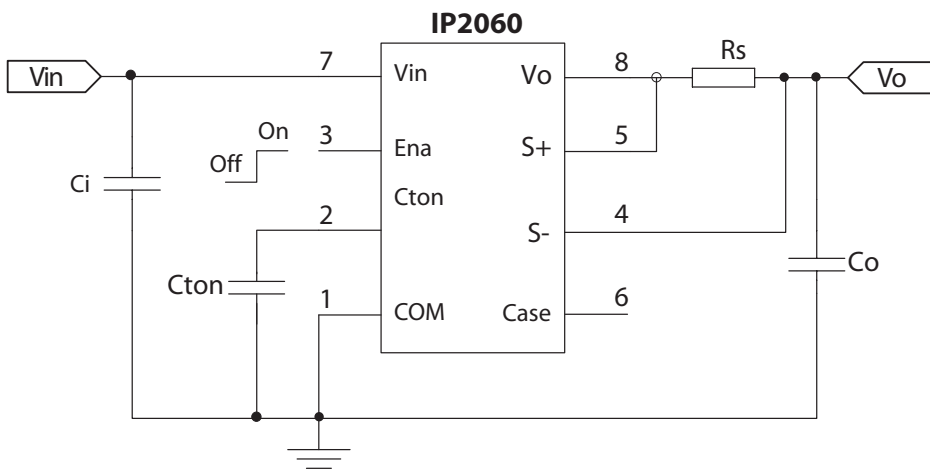
- Up to 95% efficiency for 5V version
- 6A output current
- 4.5V to 32V input range
- 2.5V, 3.3V, 5.0V fixed output versions
- 300KHz switching frequency @ 3A and above
- User programmable soft-start
- Quiescent current less than 1mA
- User programmable current limit



### DESCRIPTION

IP2060 series are high efficiency, 6A and step-down Switching regulators, making them ideal for use in military, aerospace and other high reliability applications. The output voltage is configured for 2.5V, 3.3V or 5.0V internally and the input range is 4.5V to 32V. The operating frequency of the IP2060 is 300KHz and is internally set. An external "soft start" capacitor allows the user to control how quickly the output comes up to regulation voltage after the application of an input. An extremely low quiescent current of typically less than 1mA and 95% operating efficiency keeps the total internal power dissipation of the IP2060 down to an absolute minimum. IP2060 series adopts thick-film hybrid techniques and are packaged in hermetically sealed metal cases.

### TYPICAL APPLICATION



Where:  $C_o = 5 * 330 \mu\text{f} + 0.1 \mu\text{f}$ ,

$C_{in} = 6 * 10 \mu\text{f} + 0.1 \mu\text{f}$ ,

C is "SOFT START Capacitance"

### ABSOLUTE MAXIMUM RATINGS

Vin Input Voltage	-0.3V,+32V	Tst Storage Temperature Range	-65°C ~ +150°C
VEN Enable Voltage	-0.3V,+32V	Tld Lead Temperature Range(10s)	300°C
Iout Output Current	6.0 A	Tc Operating Temperature	-55°C ~ +105°C
Sense pin voltage	-0.3V,+7V	Tj Junction Temperature	+150°C

### ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	GROUP SUBGROUP	MIN	TYP	MAX	UNITS
Input Voltage		1,2,3	4.5	-	32	V
IP2060-2.5M	Iout=1A Vin=5.0V	1,2,3	2.47	2.5	2.53	V
IP2060-3.3M	Iout=1A Vin=5.0V	1,2,3	3.27	3.3	3.37	V
IP2060-5.0M	Iout=1A Vin=6.5V	1,2,3	4.90	5.0	5.10	V
Output Current		1	-	6	-	A
Load Regulation	Output not current limited	1,2,3	-	-	2	%
Line Regulation	Iout=1A 6V≤Vin≤32V	1,2,3	-	-	1	%
Static State Power Dissipation <sup>1</sup>	Iout = 0mA	-	-	10	-	mW
Oscillator Frequency <sup>1</sup>	Iout ≥ 1.5A	-	-	300	-	KHz
Enable Input Voltage <sup>1</sup>	High	1,2,3	2.0	-	-	V
	Low	1,2,3	-	-	0.5	V
Enable Input Current <sup>1</sup>	V <sub>en</sub> = Vin	1	-	-	2.0	uA
Current Limits Threshold <sup>1</sup>	Positive	1	-	75	-	mV
Efficiency	IP2060-2.5	Vin=4.5V Iout=3A	1	-	85	%
	IP2060-3.3	Vin=5.0V Iout=3A	1	-	90	%
	IP2060-5.0	Vin=6.0V Iout=3A	1	-	95	%

### NOTES

1. Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
2. Group Subgroup: 1: Tc=25°C test : 2: Tc=-55°C: 3: Tc =+105°C

## APPLICATION NOTES

### Current Limiting

RSENSE's choice based on the requirement of output current. The current-limit circuit resets the main PWM latch and turns off the internal high-side MOSFET switch whenever the voltage exceeds Sense High and Sense Low 75mV. Allowing a margin for variations and external resistance values y

$$R_{SENSE} = \frac{50mV}{I_{max}}$$

For very high-current applications, it may be useful to wire the sense inputs with a twisted-pair instead of PCB traces. This twisted-pair needn't be anything unique, perhaps two pieces of wire-wrap wire twisted together. Low inductance current sense resistors, such as metal film surface mount styles are best.

### Soft Start/Cton

The internal soft-start circuitry allows a gradual increase of the internal current-limit level at start-up for the purpose of reducing input surge currents, and possibly for power-supply sequencing. Capacitor Cton control this function which put between PIN3 and GND. When Enable goes high, a 0.1mA current source charges the Cton capacitor up to 3.0V. The result linear ramp causes the internal current-limit threshold to increase proportionally from 25mV to 75mV. The output capacitors charge up relatively slowly, depending on the Cton capacitor value.

$$T_{DELAY} = \frac{1.5V}{0.1mA} \times (C_{ton} + C_{nei}) = 15ms/\mu F \times (C_{ton} + C_{nei})$$

and Cton parallel connected, ceramic capacitor as preferable options.

### Enable Function

The IP2060 is enabled by applying a logic level high to the Enable pin. A logic level low will disable the device and quiescent input current will reduce to approximately 2mA. The Enable threshold voltage is 1.5V. If automatic start up is required, simply connect the pin to VIN. Maximum Enable voltage is +36V.

### Power Dissipation

In high current application, it is very important to ensure that all MOSFETS are within their maximum junction temperature at environment of high temperature. Temperature rise can be calculated based on package thermal resistance and worst case dissipation for each MOSFET. These worst case dissipations occur at minimum voltage for the high side MOSFET and at maximum voltage for the low side MOSFET.

Calculate power dissipation using the following formulas:

- 1) Main switch(High FET)

on-dissipation 
$$P_{cd} = \frac{V_{out}}{V_{in}} I_{load}^2 R_{ds} = \frac{3.3}{5} \times 6^2 \times 0.009 = 0.214W$$

Switching dissipation 
$$P_{sw} = \frac{1}{2} \times V_{in} \times (tr + tf) \times fs \times I_{load} = 5 \times 25 \times 10^{-9} \times 300 \times 10^3 \times 6 = 0.225W$$

typical capacitance dissipation

$$P_{cs} = Q_{gs} V_{gs} fs = 6.7 \times 10^{-9} \times 5 \times 300 \times 10^3 = 0.01W$$

Total dissipation: 0.449W

- 2) Low FET

$$P_{cd} = \left(1 - \frac{V_{out}}{V_{in}}\right) I_{load}^2 R_{ds} = \left(1 - \frac{3.3}{5}\right) \times 6^2 \times 0.009 = 0.29W$$

## APPLICATION NOTES CONTINUED

### Heat Sinking

A heat sinking with large enough must be used in testing or application to maintain case temperature under 125°C to avoid destruction.

### Input Capacitors Selection

To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. RMS input ripple current is determined by the input voltage and load current, with the worst possible case occurring at  $V_{IN} = 2 \times V_{OUT}$ , The maximum RMS capacitor current is given by:

$$I_{rms} = I_{load} \times \frac{\sqrt{V_{out}(V_{in} - V_{out})}}{V_{in}} \quad V_{in} = 2 \times V_{out}, I_{rms \text{ max}}$$

This makes it advisable to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

### Output Capacitor Selection

The selection of  $C_{OUT}$  is primarily determined by the effective series resistance (ESR) to minimize voltage ripple, The capacitor must meet minimum capacitance and maximum ESR values as given in the following equations:

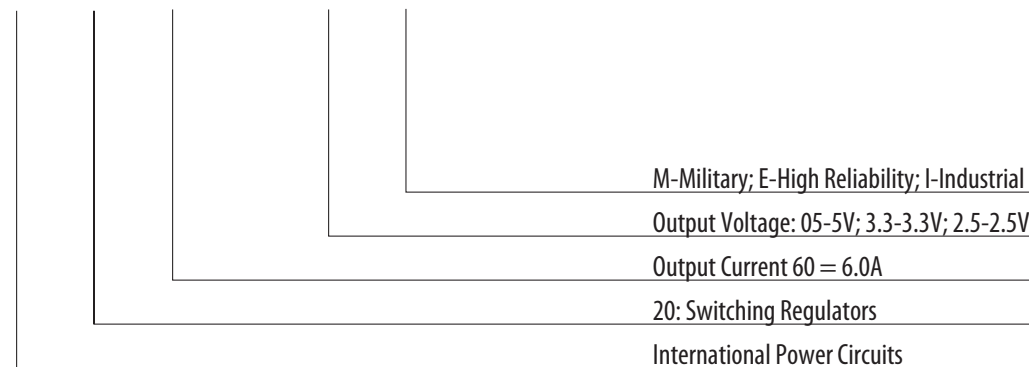
$$C_o \geq \frac{\Delta I}{8fs\Delta V_o} \quad ESR \leq \frac{\Delta V_o}{\Delta I_{load}}$$

### Modes of Operation

At light loads, the IP2060 goes into idle mode, skipping most of the oscillator pulses in order to reduce the switching frequency and cut back gate-charge losses.

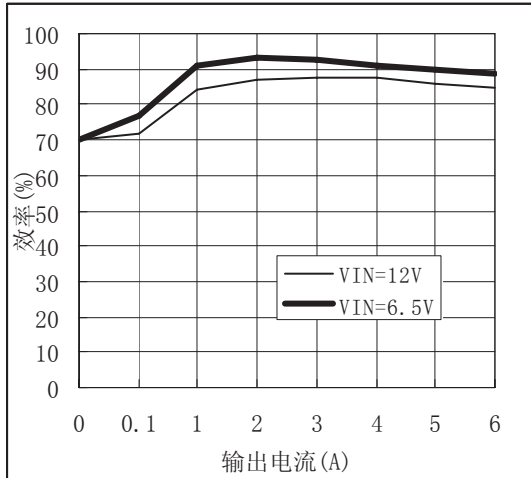
## ORDERING INFORMATION

**IP 20 60 - 3.3 M**

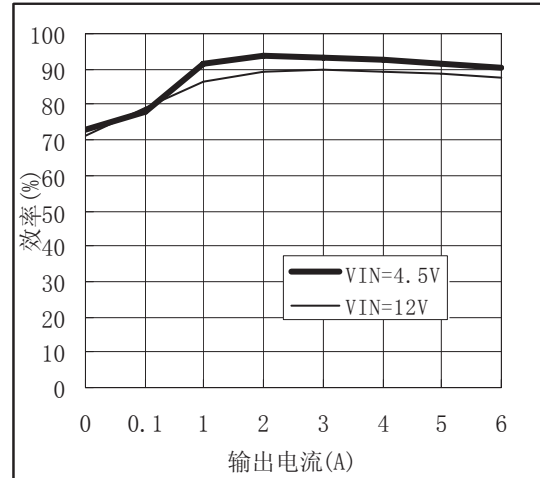


**TYPICAL PERFORMANCE CURVES**

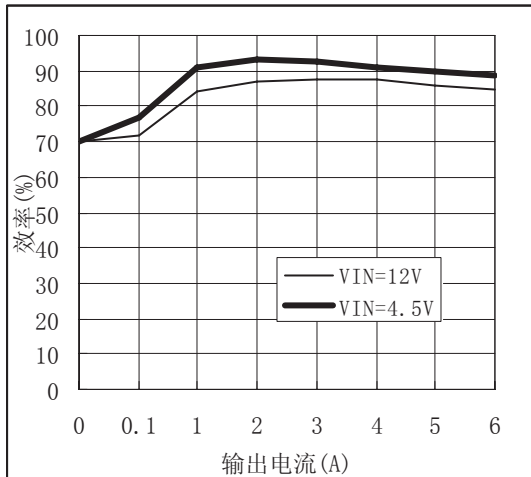
**IP2060-5.0**



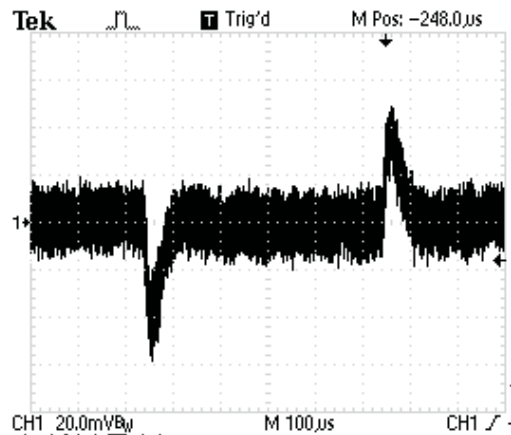
**IP2060-3.3**



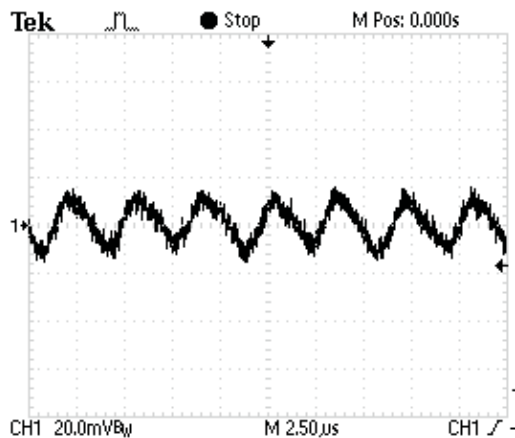
**IP2060-2.5**



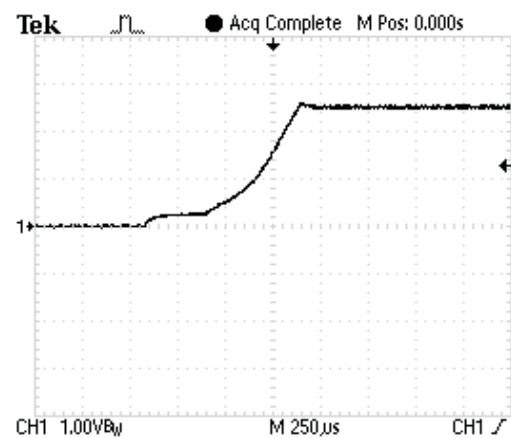
**50%~75% transient response**



**Output ripple**



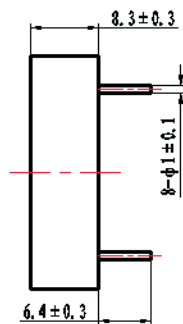
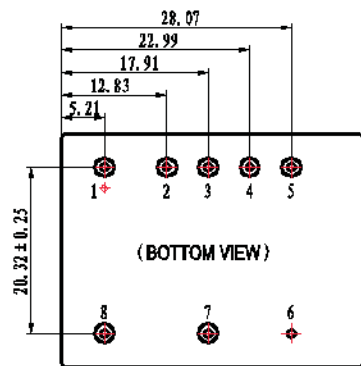
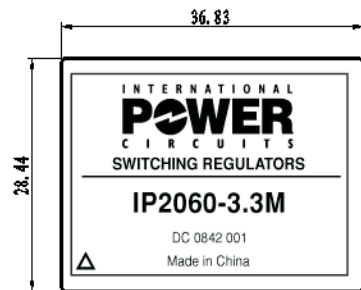
**Start time**



## ENVIRONMENTAL SCREENING

TEST ITEM	MIL-STD-883 & METHOD	CONNDITION	M	E	I
Internal Visual	2010	-	100%	100%	100%
High Temperature Bake	1008	150°C, 24h	100%	100%	-
Temp-Cycle	1010	-65°C ~+150°C 10Times	100%	100%	-
Constant Acceleration	2001	3000g, Y1 orientation	100%	100%	-
Burn In Test	1015	+125°C, 160h	100%	-	-
		+125°C, 48h	-	100%	100%
Final electrical test	-	+25°C	100%	100%	100%
		+125°C	100%	100%	-
		-55°C	100%	100%	-
Seal	1014	A1 & C1	100%	100%	100%
External Inspection	2009	-	100%	100%	100%

## PACKAGE



PIN FUNCTIONS		PIN
COMMON	COM	1
CONTROL	CON	2
ENABLE	ENA	3
CURRENT SENSE-	S-	4
CURRENT SENSE+	S+	5
CASE	CASE	6
INPUT+	VIN+	7
OUTPUT+	Vout	8

## MARKING SPECIFICATION

Serial Number: DC 0821 001, example indicates this product has been manufactured in the 21st week of 2008, and the sequence number is 001.